Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A registered buffer chip comprising:

a mode signal that indicates a muxed mode and a non-muxed mode;

a differential clock input for receiving a differential clock signal;

a slave clock buffer, receiving the differential clock signal, for generating a continuous slave clock that pulses during both the muxed mode and during the non-muxed mode;

a first master clock buffer, receiving the differential clock signal, for generating a first clock that pulses during the non-muxed mode but does not pulse during the muxed mode;

a second master clock buffer, receiving the differential clock signal, for generating a second clock that pulses during the muxed mode but does not pulse during the non-muxed mode;

a dual-bit slice that comprises:

a first data input;

a first data buffer, receiving the first data input, for driving a first internal data signal;

a second data input;

a second data buffer, receiving the second data input, for driving a second internal data signal;

a first muxed flip-flop receiving the first internal data signal as a first mux input and the second internal data signal as a second mux input, for generating a first data output;

a second muxed flip-flop receiving the second internal data signal as both the first mux input and as the second mux input, for generating a second data output;

wherein the first muxed flip-flop and the second muxed flip-flop each comprise a muxed master stage and a slave stage;

wherein the muxed master stage comprises:

a first transmission gate that conducts between the first mux input and a master node in response to the first clock;

a second transmission gate that conducts between the second mux input and a master node in response to the second clock;

a master inverting gate, having the master node as an input, for driving a coupled node;

a master feedback gate, receiving the first clock and the second clock, and having the coupled node as an input, for driving the master node when neither the first transmission gate nor the second transmission gate are conducting;

wherein the slave stage comprises:

a slave transmission gate that conducts between the coupled node and a slave node in response to the slave clock;

a slave inverting gate, having the slave node as an input, for driving an output node; and

a slave feedback gate, receiving the slave clock, and having the output node as an input, for driving the slave node when the slave transmission gate is not conducting,

whereby the muxed master stage has muxed inputs clocked by mode-enabled clocks so that the first data output but not the second data output is muxed during the muxed mode.

[c2] 2.The registered buffer chip of claim 1 wherein the master feedback gate comprises:

a first feedback p-channel transistor having a gate receiving the coupled node;

a second feedback p-channel transistor having a gate receiving an inverse of the second clock;

a third feedback p-channel transistor having a gate receiving an inverse of the first clock;

a first feedback n-channel transistor having a gate receiving the coupled node;

a second feedback n-channel transistor having a gate

receiving the second clock;
a third feedback n-channel transistor having a gate receiving the first clock;
wherein the first, second, and third feedback p-channel transistors are in series between a power supply and the master node;
wherein the first, second, and third feedback n-channel transistors are in series between a ground and the master node.

[c3] 3.The registered buffer chip of claim 2 wherein the first transmission gate comprises an n-channel transistor having a gate receiving the inverse of the first clock and a p-channel transistor receiving the first clock;
wherein the second transmission gate comprises an n-channel transistor having a gate receiving the inverse of the second clock and a p-channel transistor receiving the second clock.

[c4] 4.The registered buffer chip of claim 3 wherein the slave feedback gate comprises:
a first slave feedback p-channel transistor having a gate receiving the output node;
a second slave feedback p-channel transistor having a gate receiving the slave clock;
a first slave feedback n-channel transistor having a gate receiving the output node;

a second slave feedback n-channel transistor having a gate receiving an inverse of the slave clock;
wherein the first and second slave feedback p-channel transistors are in series between the power supply and the slave node;
wherein the first and second slave feedback n-channel transistors are in series between the ground and the slave node.

[c5] 5.The registered buffer chip of claim 4 wherein the slave transmission gate comprises an n-channel transistor having a gate receiving the slave clock and a p-channel transistor receiving the inverse of the slave clock.

[c6] 6.The registered buffer chip of claim 1 further comprising a plurality of the dual-bit slices, each dual-bit slice in the plurality of dual-bit slices coupled to a different pair of data input signals, and each generating a different pair of first and second data outputs,
whereby multiple dual-bit slices are in the registered buffer chip and every other bit is muxed during the muxed mode.

[c7] 7.The registered buffer chip of claim 6 wherein the first data buffer comprises a differential buffer that receives the first internal data signal and a reference voltage, the first data buffer comparing a voltage of the first internal

data signal to the reference voltage to generate the first internal data signal;

wherein the second data buffer comprises a differential buffer that receives the second data signal and a reference voltage, the second data buffer comparing a voltage of the second data signal to the reference voltage to generate the second internal data signal.

[c8] 8.The registered buffer chip of claim 6 wherein the output node of the first muxed flip-flop is the first data output, or the output node is buffered to generate the first data output;

wherein the output node of the second muxed flip-flop is the second data output, or the output node is buffered to generate the second data output.

[c9] 9.The registered buffer chip of claim 6 wherein the slave inverting gate is a NOR gate or a NAND gate receiving a reset signal,

whereby the slave stage is resetable.

[c10] 10.The registered buffer chip of claim 6 wherein the master inverting gate is an inverter or a NAND gate or a NOR gate.

[c11] 11.The registered buffer chip of claim 6 wherein the slave clock is a differential clock generated by the slave

clock buffer, having a true slave clock and a complement slave clock driven to the slave stages;
wherein the first clock is a differential clock generated by the first master clock buffer, having a true first clock and a complement first clock driven to the muxed master stages;
wherein the second clock is a differential clock generated by the second master clock buffer, having a true second clock and a complement second clock driven to the muxed master stages,
whereby differential clocks are driven to the first and second muxed flip-flops.

[c12] 12.A data register comprising:
a first input buffer receiving a first data input and generating a first data signal;
a second input buffer receiving a second data input and generating a second data signal;
a slave clock buffer receiving a differential clock, and pulsing a slave clock in both a muxed mode and in a pass-through mode;
a first clock buffer receiving the differential clock, and pulsing a first clock in the pass-through mode but not pulsing the first clock in the muxed mode;
a second clock buffer receiving the differential clock, and pulsing a second clock in the muxed mode but not puls-

ing the second clock in the pass-through mode;

a first master circuit comprising:

a first transmission gate clocked by the first clock, for sampling the first data signal to a master node;

a second transmission gate clocked by the second clock, for sampling the second data signal to the master node;

an inverter from the master node to a coupled node;

a feedback gate having the coupled node, the first clock, and the second clock as inputs, driving the master node when the first and second transmission gates are closed;

a first slave circuit comprising:

a slave transmission gate clocked by the slave clock, for sampling the coupled node to a slave node;

a slave gate from the slave node to a second slave node;

a slave feedback gate having the coupled node and the slave clock as inputs, driving the slave node when the slave transmission gate is closed;

wherein a first output from the slave is generated from the second slave node or from the slave node; and

a second flip-flop having a master that receives the second data signal but not the first data signal, and a slave that generates a second output in response to the slave clock,

whereby the first output is muxed from sampling either the first or second data signals, but the second output is generated from the second data signal and not the first

data signal.

[c13] 13.The data register of claim 12 wherein the master feedback gate comprises:
a first feedback p-channel transistor having a gate receiving the coupled node;
a second feedback p-channel transistor having a gate receiving an inverse of the second clock;
a third feedback p-channel transistor having a gate receiving an inverse of the first clock;
a first feedback n-channel transistor having a gate receiving the coupled node;
a second feedback n-channel transistor having a gate receiving the second clock;
a third feedback n-channel transistor having a gate receiving the first clock;
wherein the first, second, and third feedback p-channel transistors are in series between a power supply and the master node;
wherein the first, second, and third feedback n-channel transistors are in series between a ground and the master node.

[c14] 14.The data register of claim 13 wherein the first transmission gate comprises an n-channel transistor having a gate receiving the inverse of the first clock and a p-channel transistor receiving the first clock;

wherein the second transmission gate comprises an n-channel transistor having a gate receiving the inverse of the second clock and a p-channel transistor receiving the second clock.

[c15] 15.The data register of claim 14 wherein the slave feedback gate comprises:
a first slave feedback p-channel transistor having a gate receiving the second slave node;
a second slave feedback p-channel transistor having a gate receiving the slave clock;
a first slave feedback n-channel transistor having a gate receiving the second slave node;
a second slave feedback n-channel transistor having a gate receiving an inverse of the slave clock;
wherein the first and second slave feedback p-channel transistors are in series between the power supply and the slave node;
wherein the first and second slave feedback n-channel transistors are in series between the ground and the slave node.

[c16] 16.The data register of claim 15 wherein the slave transmission gate comprises an n-channel transistor having a gate receiving the slave clock and a p-channel transistor receiving the inverse of the slave clock.

[c17] 17.The data register of claim 12 further comprising a plurality of dual-bit slices, each dual-bit slice in the plurality of dual-bit slices having a first master circuit and a first slave circuit and a second flip-flop, each of the plurality of dual-bit slices coupled to a different pair of data input signals, and each generating a different pair of first and second data outputs,
whereby every other bit is muxed during the muxed mode.

[c18] 18.The data register of claim 17 wherein the first input buffer comprises a differential buffer that receives the first data signal and a reference voltage, the first input buffer comparing a voltage of the first data signal to the reference voltage to generate the first data signal;
wherein the second input buffer comprises a differential buffer that receives the second data signal and a reference voltage, the second input buffer comparing a voltage of the second data signal to the reference voltage to generate the second data signal.

[c19] 19.The data register of claim 18 wherein the slave clock is a differential clock generated by the slave clock buffer, having a true slave clock and a complement slave clock driven to the first slave circuit;
wherein the first clock is a differential clock generated by the first clock buffer, having a true first clock and a

complement first clock driven to the first master circuit;
wherein the second clock is a differential clock generated by the second clock buffer, having a true second clock and a complement second clock driven to the first master circuit,
whereby differential clocks are internally driven.

[c20] 20.A registered memory module buffer chip comprising:
mode signal means for indicating a muxed mode and a non-muxed mode;
a differential clock input for receiving a differential clock signal;
slave clock buffer means, receiving the differential clock signal, for generating a slave clock that pulses during both the muxed mode and during the non-muxed mode;
first master clock buffer means, receiving the differential clock signal, for generating a first clock that pulses during the non-muxed mode but does not pulse during the muxed mode;
second master clock buffer means, receiving the differential clock signal, for generating a second clock that pulses during the muxed mode but does not pulse during the non-muxed mode;
a dual-bit slice that comprises:
a first data input;
a first data buffer means, receiving the first data input,

for driving a first internal data signal;
a second data input;
a second data buffer means, receiving the second data input, for driving a second internal data signal;
first muxed flip-flop means, receiving the first internal data signal as a first mux input and the second internal data signal as a second mux input, for generating a first data output;
second muxed flip-flop means, receiving the second internal data signal as both the first mux input and as the second mux input, for generating a second data output;
wherein the first muxed flip-flop means and the second muxed flip-flop means each comprise a master stage and a slave stage;
wherein the master stage comprises:
first transmission gate means for conducting between the first mux input and a master node in response to the first clock;
second transmission gate means for conducting between the second mux input and a master node in response to the second clock;
master inverting gate means, having the master node as an input, for driving a coupled node;
master feedback gate means, receiving the first clock and the second clock, and having the coupled node as an input, for driving the master node when neither the first

transmission gate means nor the second transmission gate means are conducting;

wherein the slave stage comprises:

slave transmission gate means for conducting between the coupled node and a slave node in response to the slave clock;

slave inverting gate means, having the slave node as an input, for driving an output node; and

slave feedback gate means, receiving the slave clock, and having the output node as an input, for driving the slave node when the slave transmission gate means is not conducting,

whereby the master stage has muxed inputs clocked by mode-enabled clocks so that the first data output but not the second data output is muxed during the muxed mode.